

Course Manual ESY

Embedded Systems in Media Technology

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– General information

Long name Embedded Systems in Media Technology

Approving CModule [ESY_MaMT](#)

Responsible Prof. Dr.-Ing. Dirk Poggemann
Professor Fakultät IME

Valid from winter semester 2020/21

Level Master

Semester in the year winter semester

Duration Semester

Hours in self-study 78

ECTS 5

Professors Prof. Dr.-Ing. Dirk Poggemann
Professor Fakultät IME

Requirements none

Language German, English if necessary

Separate final exam Yes

Literature

H.Flügel, FPGA-Design mit Verilog, Oldenbourg

D.G.Bailey, Design for Embedded Image Processing on FPGAs, Wiley

F.Kesel, Entwurf von digitalen Schaltungen und Systemen mit HDLs und FPGAs, Oldenbourg

Final exam

Details Students implement media technology algorithms in an Embedded System and document their results. The Implementation should be developed and tested as introduced in the lecture and the lab exercises.

Minimum standard Working Algorithm

Exam Type EN schriftlicher Ergebnisbericht

– Lecture / Exercises

Learning goals

Goal type	Description
Knowledge	<ul style="list-style-type: none">- Microprocessors- FPGAs- Hardware Description Languages- Designprocess- Test and Debug- Control of CCD- and CMOS-Image-Sensors- Image Processing Algorithms

Special requirements

none

Accompanying material	electronic slides as presented during lectures
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Separate exam	No
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Expenditure classroom teaching

Type	Attendance (h/Wk.)
Lecture	2
Tutorial (voluntary)	0

– Practical training

Learning goals

Goal type	Description
Skills	exercises with FPGA-Board and CMOS-Image-Sensor

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Practical training	2
Tutorial (voluntary)	0

Special requirements

none

Accompanying material electronic description of lab-exercises

Separate exam Yes

Separate exam

Exam Type EN praxisnahes Szenario bearbeiten (z.B. im Praktikum)

Details Reports about lab exercises

Minimum standard Reports for all lab exercises must be delivered in correct form with correct results