Technology
Arts Sciences
TH Köln

Course Manual SOP

Systems on Programmable Chips

Version: 1 | Last Change: 02.08.2019 14:22 | Draft: 0 | Status: vom verantwortlichen Dozent freigegeben

General information

Long name	Systems on Programmable Chips
Approving CModule	SOP_BaTIN
Responsible	Prof. Dr. Tobias Krawutschke Professor Fakultät IME
Valid from	summer semester 2022
Level	Bachelor
Semester in the year	summer semester
Duration	Semester
Hours in self-study	78
ECTS	5
Professors	Prof. Dr. Tobias Krawutschke Professor Fakultät IME

Literature

Hamblen, Furman: Rapid Prototyping of Digital Systems, Kluwer Academic Publishing

Wakerly: Digital Design: Principles and Practices, Prentice Hall

D. Gajski: Embedded System Design, Springer Verlag New York

U. Meyer-Baese: Digital Signal Processing with Field Programmable Gate Arrays

Final exam

Details	Preparation part: Analysis of a typical task suited for SoPC, Design of a solution (Student alone in examination context) Discussion part: disputation of solution, crafting of selected parts (student under supervision of docent)
Minimum standard	Derivation of important system components and correct mapping to hardware Ability to implement selected components (HW/SW)

Requirements	Fundamentals of digital systems * Design Methods (Boolean Algebra, Automata) * Basic knowledge of digital technology including hardware description language Fundamentals Programming * Hardwareoriented Programming with C * Programming experience * Knowledge and first experiences in reactive programming, especially using interrupts Fundamentals of signal processing, esp. digital filters (FIR)
Language	German, English if necessary
Separate final exam	Yes

Exam Type	EN mündliche Prüfung, strukturierte Befragung

− Lecture / Exercises

Learning goals

Goal type	Description
Knowledge	1) Digital system modelling using Boolean algebra Schematic (using digital basic components) Finite State Automata (FSA) Extended FSA, Statecharts Controlflow/Dataflow systems VHDL 2) Digital technology Understanding of typical digital circuits (CMOS technology) Understanding, description and classification of runtime effects Knowledge and variants of programmable units (PLD, FPGA) 3) SoC/SoPC-Systeme System construction IO access using machine-near programming Interrupts, alarm Programming automata / CFDF systems Rules to partition hardware and software components Design of coupling of HW/SW components

Special requirements

none

Accompanying material	Course slides Exercise task sheets with solutions Tutorials Example models and programs
Separate exam	No

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Lecture	2
Exercises (whole course)	1
Exercises (shared course)	0
Tutorial (voluntary)	2

− Practical training

Learning goals

Goal type	Description
Skills	Getting compentencies in analysis, modelling and implementation of the hardware part of an audio signal processing system 1) Analysis of interface to the CoDec and creation of a system reading in and writing out samples (copy-machine) 2) Development of a FIR filter working on the samples 3) Development of a simple echo producer working in the time domain
Skills	Getting compentencies in analysis, modelling and implementation of an audio signal processing system in software 1) Analysis of interface to the CoDec and creation of a system reading in and writing out samples (copy-machine) 2) Development of a N-stage averaging mean filter working on the samples 3) Development of a simple echo producer working in the time domain 4) Measurement and optimization of the system since it reaches the performance limit of standard microcontrollers
Skills	Realization of the example system as a HW/SW system with input of parameter values for echo and FIR filter unit 1) System partition HW/SW 2) Protocoll specification between HW and SW components 3) Realization of User Interface (Input of echo and filter parameters, general system control) 4) Realization of protocoll components 5) Validation with FPGA Board 6) Comparison of solutions HW / SW / SoPC in report

Expenditure classroom teaching

Special requirements

none

Accompanying material	Textual description Tutorials Adapted tools e.g. for testing
Separate exam	Yes

Separate exam

Exam Type	EN praxisnahes Szenario bearbeiten (z.B. im Praktikum)
Details	Check of electronically delivered preparations (design files, models, software) Observation of lab work on a real FPGA system
Minimum standard	Delivery of all required elements in time Sufficient Quality of delivered elements Explanation of components during the lab date Participation in the implementaiton of the systems Report sufficiently elaborated

Type	Attendance (h/Wk.)
Practical training	1
Tutorial (voluntary)	0