Technology
Arts Sciences
TH Köln

Course
DR - Digital Computer

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General information

Long name	Digital Computer
Approving CModule	DR_BaTIN
Responsible	Prof. Dr. Lothar Thieling Professor Fakultät IME
Level	Bachelor
Semester in the year	winter semester
Duration	Semester
Hours in self-study	60
ECTS	5
Professors	NF Hartung
Requirements	none
Language	German
Separate final exam	Yes

Final exam

Details

The students should demonstrate the following competencies in a written exam: 1.) Safe handling of concepts and mechanisms. 2.) Analysis of given digital circuits. 3.) Design of digital systems (simple networks, counters, automata) in VHDL based on given textual specifications. 4.) Implementation of high-level language constructs in assembler or vice versa.

Minimum standard

At least 50% of the total number of points

Exam Type

The students should demonstrate the following competencies in a written exam: 1.) Safe handling of concepts and mechanisms. 2.) Analysis of given digital circuits. 3.) Design of digital systems (simple networks, counters, automata) in VHDL based on given textual specifications. 4.) Implementation of high-level language constructs in assembler or vice versa.

Lecture / Exercises

Learning goals

Knowledge

boolean algebra
basic functions
axioms and laws
disjunctive normal form, minterms
conjunctive normal form, maxterms
systematic simplification

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boolean network
logic gates, tri-state buffer
description forms
boolean equation
table
KV diagram
schematic
transformations between the forms of description
analysis
synthesis (including transfer from text to problem solution)
don't-care conditions
typical networks
decoder
multiplexer
demultiplexer
adder

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number representation in computer systems
dual-code, hexadecimal-code, change of basis
two's complement
fixed point representation
floating point representation
ASCII-code

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feedback networks
flip-flops and latches
RS
D
asynchronous control
clock state control
edge triggered

registers
parallel read-write register
shift register
parallel-serial conversion
seria-parallell conversion
practice-oriented specifications
setup time
hold time
minimum puls width

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synchronous counters
the basic idea
construction using D flip-flops
analysis
synthesis
specification using VHDL
refer VHDL

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finite state machines
description of state machines using state transition diagrams (Moore)
design of state machines as a problem-solving
Implementation using VHDL

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state transition diagrams
modeling according to Moore
characteristics (determinism, completeness)

VHDL
specification of boolean networks
structure of a VHDL program (entity, port, architecture, signals, in, out)
signals (type stdlogic: 1, 0, Tri-State, Don't-Care)
signal assignment (direct implementation of boolean functions)
conditional signal assignment (direct conversion of tables)
vectors of signals
integer data type and conversion from/to signal vectors
design entry VHDL
specification of counters and finite state machines
processes and sequential instructions (process, variable, if, case, event, type)
implementation of regular counter in VHDL
implementation of finite state machines in VHDL
hierarchical VHDL-desin
packages, components, portmaps, generics

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programmable logic devices
structure
the basic idea
technology
CPLD versus FPGA
design tool
scematic design entry
basic library (gates, in, ou, buffer, mux, decoder, flip-flops)
buses
hierarchical schematics
VHDL design entry

detail refer VHL
synthesis
simulation

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structure and mode of operation of a simple computer
structure of a Von Neumann computer (registers, arithmetic logic unit, control unit, memory, buses)
mode of operation (program execution based on register transfers)
concretization of mode of operation (a minimal simulated Von Neumann computer)
programming the minimal computer in assembler (simple loops, different addressing modes)

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design and operation of a dedicated CPU (eg IA32E-architecture)
architectural overview
mode of operation (program execution based on register transfers)
basics for programming in assembly language

Skills

specifying system behavior (derived from text documents)

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development of problem solutions that can be implemented with boolean networks

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interpretation and convertion of codes

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development of problem solutions that can be implemented with synchronous counters

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development of problem solutions that can be implemented with finite state machines

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explain the operation of a Von Neumann computer

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Lecture	2
Exercises (whole course)	1
Exercises (shared course)	1
Tutorial (voluntary)	0

Separate exam

none

Practical training

Learning goals

Skills

development od digital systems

explain the system behavior of a Von Neumann computer

implement subsystems of a Von Neumann computer

implementation of C-code sequences using assembler

manage complex tasks as a small team

develop problem solutions

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Practical training	1
Tutorial (voluntary)	0

Separate exam

none