Technology
Arts Sciences
TH Köln

Course
SOP - Systems on Programmable Chips

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General information

Long name	Systems on Programmable Chips
Approving CModule	SOP_BaTIN
Responsible	Prof. Dr. Tobias Krawutschke Professor Fakultät IME
Level	Bachelor
Semester in the year	summer semester
Duration	Semester
Hours in self-study	78
ECTS	5
Professors	Prof. Dr. Tobias Krawutschke Professor Fakultät IME
Requirements	Fundamentals of digital systems * Design Methods (Boolean Algebra, Automata) * Basic knowledge of digital technology including hardware description language Fundamentals Programming * Hardwareoriented Programming with C * Programming experience * Knowledge and first experiences in reactive programming, especially using interrupts Fundamentals of signal processing, esp. digital filters (FIR)
Language	German, English if necessary
Separate final exam	Yes

Final exam

Details

Preparation part: Analysis of a typical task suited for SoPC, Design of a solution (Student alone in examination context)

Discussion part: disputation of solution, crafting of selected parts (student under supervision of docent)

Minimum standard

Derivation of important system components and correct mapping to hardware

Ability to implement selected components (HW/SW)

Exam Type

Preparation part: Analysis of a typical task suited for SoPC, Design of a solution (Student alone in examination context)

Discussion part: disputation of solution, crafting of selected parts (student under supervision of docent)

Lecture / Exercises

Learning goals

Knowledge

1) Digital system modelling using

Boolean algebra

Schematic (using digital basic components)

Finite State Automata (FSA)

Extended FSA, Statecharts

Controlflow/Dataflow systems

VHDL

2) Digital technology

Understanding of typical digital circuits (CMOS technology)

Understanding, description and classification of runtime effects

Knowledge and variants of programmable units (PLD, FPGA)

3) SoC/SoPC-Systeme

System construction

IO access using machine-near programming

Interrupts, alarm

Programming automata / CFDF systems

Rules to partition hardware and software components

Design of coupling of HW/SW components

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Lecture	2
Exercises (whole course)	1
Exercises (shared course)	0

Tutorial (voluntary)	2

Separate exam

none

Practical training

Learning goals

Skills

Getting compentencies in analysis, modelling and implementation of the hardware part of an audio signal processing system
1) Analysis of interface to the CoDec and creation of a system reading in and writing out samples (copy-machine)
2) Development of a FIR filter working on the samples
3) Development of a simple echo producer working in the time domain

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Getting compentencies in analysis, modelling and implementation of an audio signal processing system in software
1) Analysis of interface to the CoDec and creation of a system reading in and writing out samples (copy-machine)
2) Development of a N-stage averaging mean filter working on the samples
3) Development of a simple echo producer working in the time domain
4) Measurement and optimization of the system since it reaches the performance limit of standard microcontrollers

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Realization of the example system as a HW/SW system with input of parameter values for echo and FIR filter unit
1) System partition HW/SW
2) Protocoll specification between HW and SW components
3) Realization of User Interface (Input of echo and filter parameters, general system control)
4) Realization of protocoll components
5) Validation with FPGA Board
6) Comparison of solutions HW / SW / SoPC in report

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Practical training	1
Tutorial (voluntary)	0

Separate exam

Exam Type

working on practical scenarion (e.g. in a lab)

Details

Check of electronically delivered preparations (design files, models, software)

Observation of lab work on a real FPGA system

Minimum standard

Delivery of all required elements in time

Sufficient Quality of delivered elements

Explanation of components during the lab date

Participation in the implementaiton of the systems

Report sufficiently elaborated