Technology
Arts Sciences
TH Köln

Course
DSF - Digital Signal Processing with FPGA

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General information

Long name	Digital Signal Processing with FPGA
Approving CModule	DSF_BaET, DSF_BaTIN
Responsible	Prof. Dr. Jens Onno Krah Professor Fakultät IME
Level	Bachelor
Semester in the year	summer semester
Duration	Semester
Hours in self-study	60
ECTS	5
Professors	Prof. Dr. Jens Onno Krah Professor Fakultät IME
Requirements	TI1, DSS, SuS
Language	German
Separate final exam	Yes

Final exam

Details

Written module examination - similar to the exercises

Minimum standard

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Exam Type

Written module examination - similar to the exercises

Lecture / Exercises

Learning goals

Skills

Basics of digital signal processing,
Time-discrete systems
Analog-to-digital conversion and sample-and-hold
Sigma delta modulation, quantization noise
Practical application of z-transformation
Design of digital filters (IIR and FIR)
fixed-point arithmetic
Implementation in a DSP environment ("C" + Assembler)
Implementation in an FPGA environment ("VHDL")
FPGA development system Quartus II
Introduction of the FPGA series Max 10 from Altera / Intel
Eclipse / Nios II development environment

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Lecture	2
Exercises (whole course)	2
Exercises (shared course)	0
Tutorial (voluntary)	0

Separate exam

none

Practical training

Learning goals

Skills

Practical application of z-transformation
Implementation in an FPGA environment ("VHDL")
FPGA development system Quartus II
Introduction of Altera's Max 10 FPGA Series / Intel
Nios II development environment

Expenditure classroom teaching

Type	Attendance (h/Wk.)
Practical training	1
Tutorial (voluntary)	0

Separate exam

none